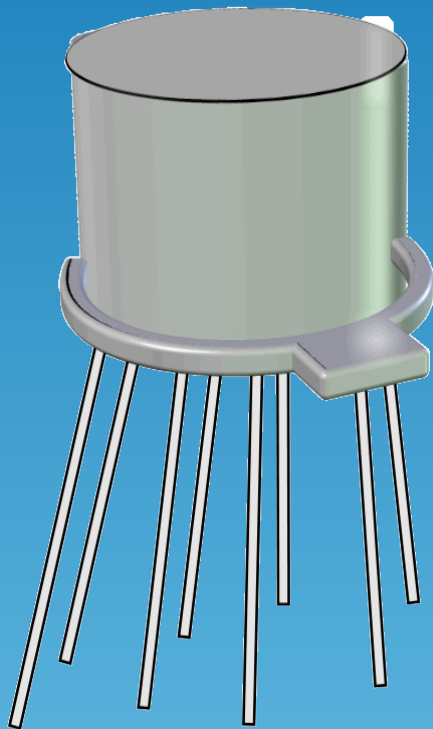
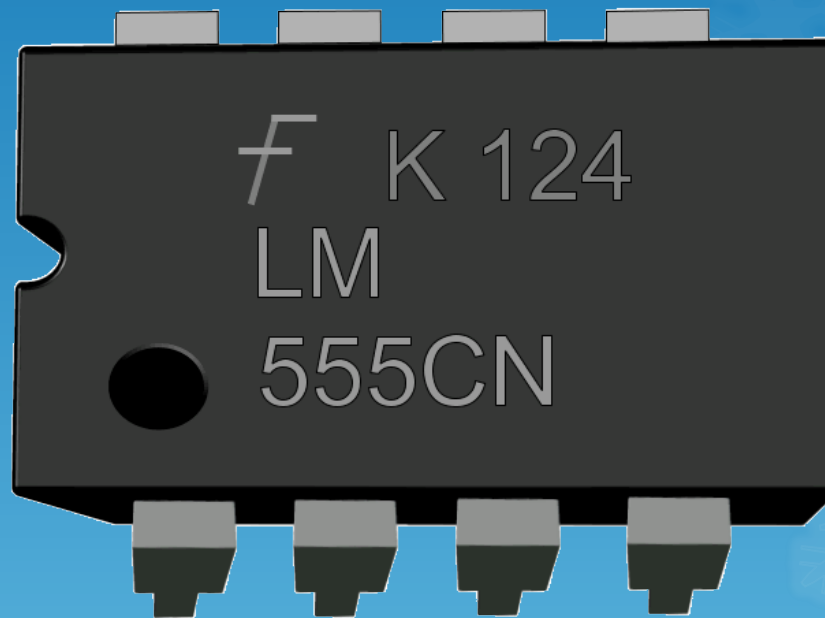


# 555 Timer Basics

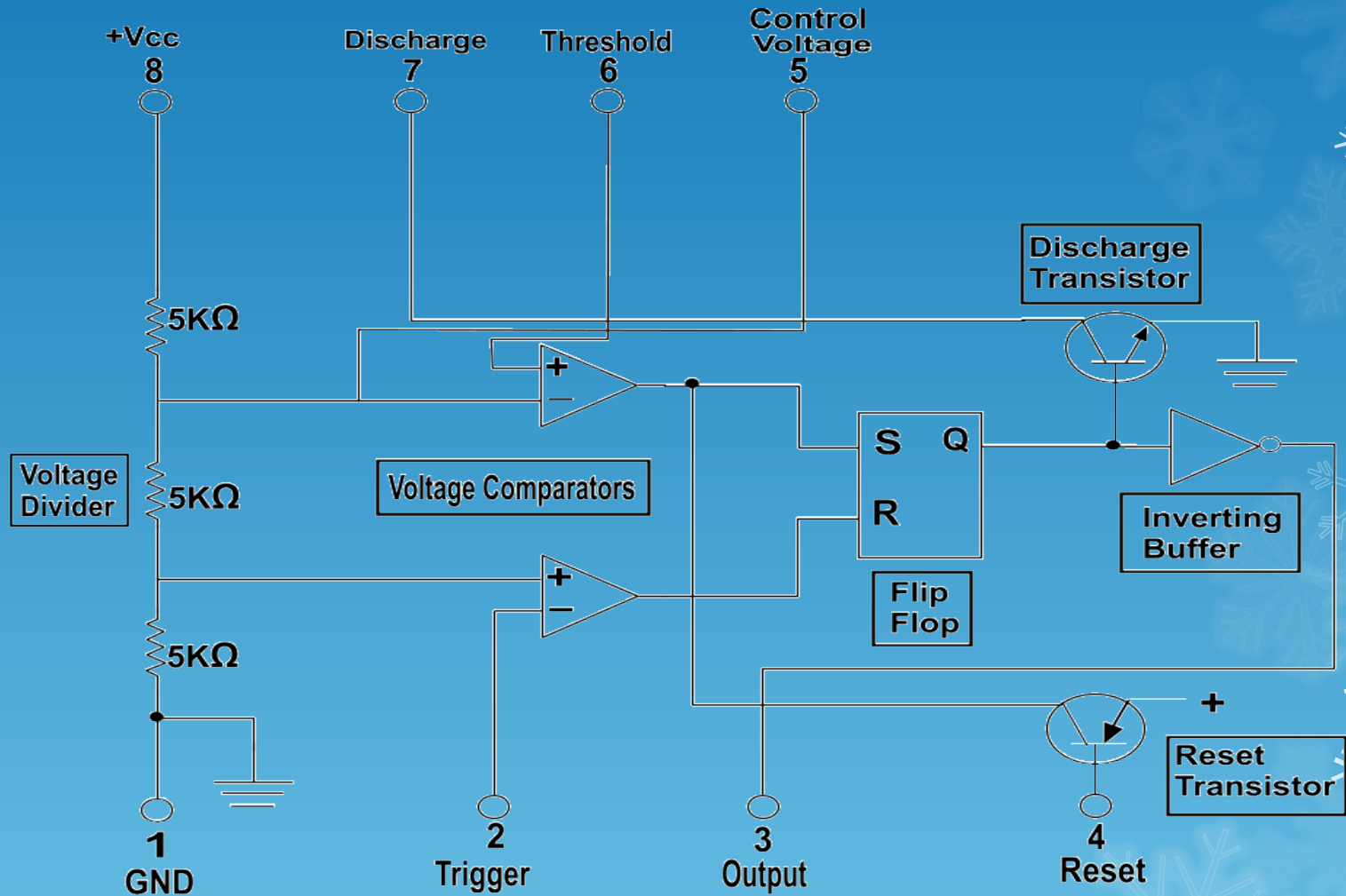


TO-5 Package

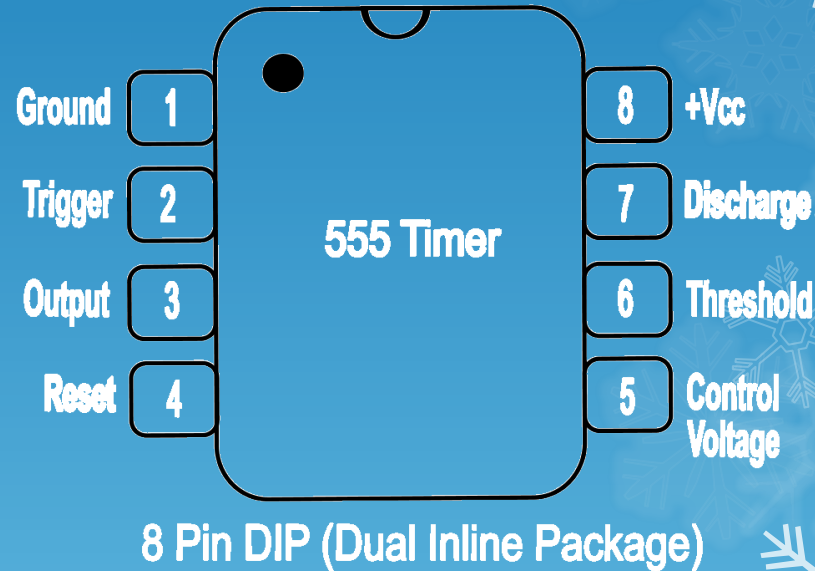
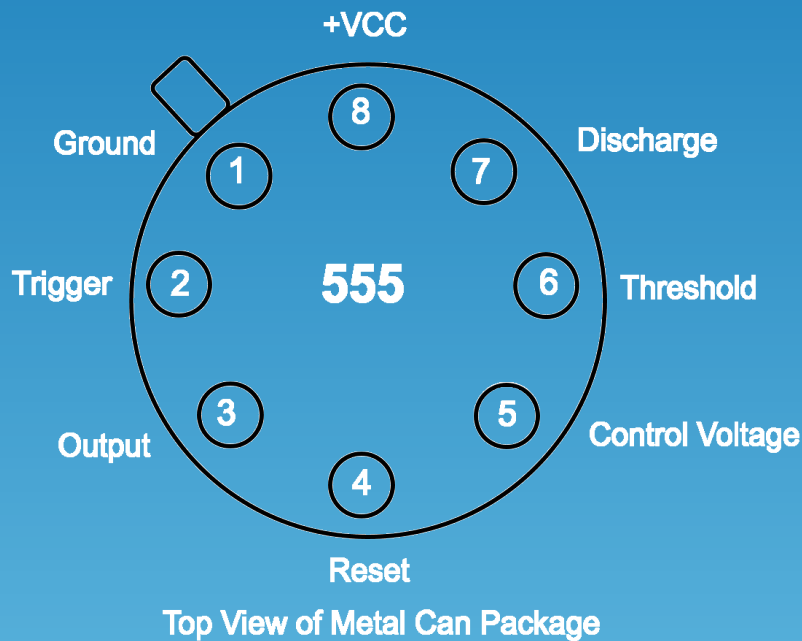


Eight-pin IC, LM555CN

# 555 Internal Construction



# 555 IC, 8 Pin Pinout Diagrams



# Explanation of Terminals for 8 pin 555

- **Pin 1: Grounded Terminal:** All the voltages are measured with respect to this terminal.

## ○ **Pin 2: Trigger Terminal:**

This pin is an inverting input to a comparator that is responsible for transition of flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.



The background is a solid blue color with several white snowflake graphics scattered across it. The snowflakes vary in size and are positioned primarily on the right side of the slide. One large snowflake is in the top right, another is in the middle right, and several others are in the bottom right area.

## ○ **Pin 3: Output Terminal:**

Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal either between pin 3 and ground pin (pin 1) or between pin 3 and supply pin (pin 8).

## Pin 3 continued...

- The load connected between pin 3 and the supply supply pin is called the ***normally on load*** and the load connected between pin 3 and ground pin is called the ***normally off load***

**○ Pin 4: Reset Terminal:** To disable or reset the timer a negative pulse is applied to this pin due to the fact it is referred to as reset terminal. When this pin is not to be used for reset purpose, it should be connected to  $+V_{CC}$  to avoid any possibility of false triggering.



## ○ Pin 5: Control Voltage

**Terminal:** The function of this terminal is to control the threshold and trigger levels. Thus either the external voltage or a pot connected to this pin determines the pulse width of the output waveform.

## Pin 5 continued...

- The external voltage applied to this pin can also be used to modulate the output waveform. When this pin is not used, it should be connected to ground through a 0.01 micro Farad to avoid any noise problem.

## ○ Pin 6: Threshold Terminal:

This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of  $\frac{2}{3} V_{CC}$ . The amplitude of voltage applied to this terminal is responsible for the set state of flip-flop.

The background is a solid blue color with several white snowflake-like graphics scattered across it. These graphics are stylized, multi-pointed shapes with intricate branching patterns, resembling snowflakes or starburst patterns. They are positioned in the upper right, middle right, and lower right areas of the slide.

## ○ **Pin 7: Discharge Terminal:**

This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground.

## Pin 7 Continued...

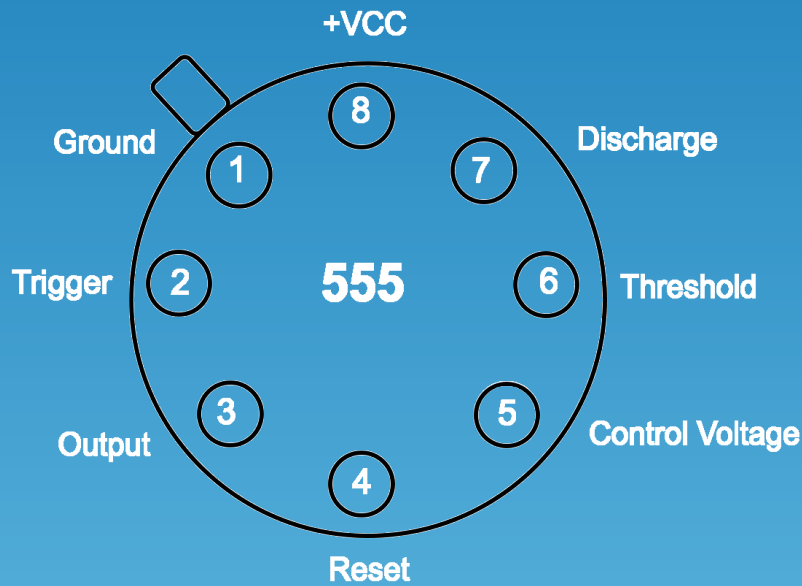
- It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. The capacitor charges at a rate determined by the external resistor and capacitor, when the transistor is cut-off.

The background is a solid blue color with several white snowflake icons scattered across it. The snowflakes vary in size and opacity, with some being more prominent than others. They are located in the top right, middle right, and bottom right areas of the slide.

## ○ Pin 8: Supply Terminal:

A supply voltage of + 5 V to + 18 V is applied to this terminal with respect to ground (pin 1).

# 555 IC, 8 Pin Pinout Diagrams

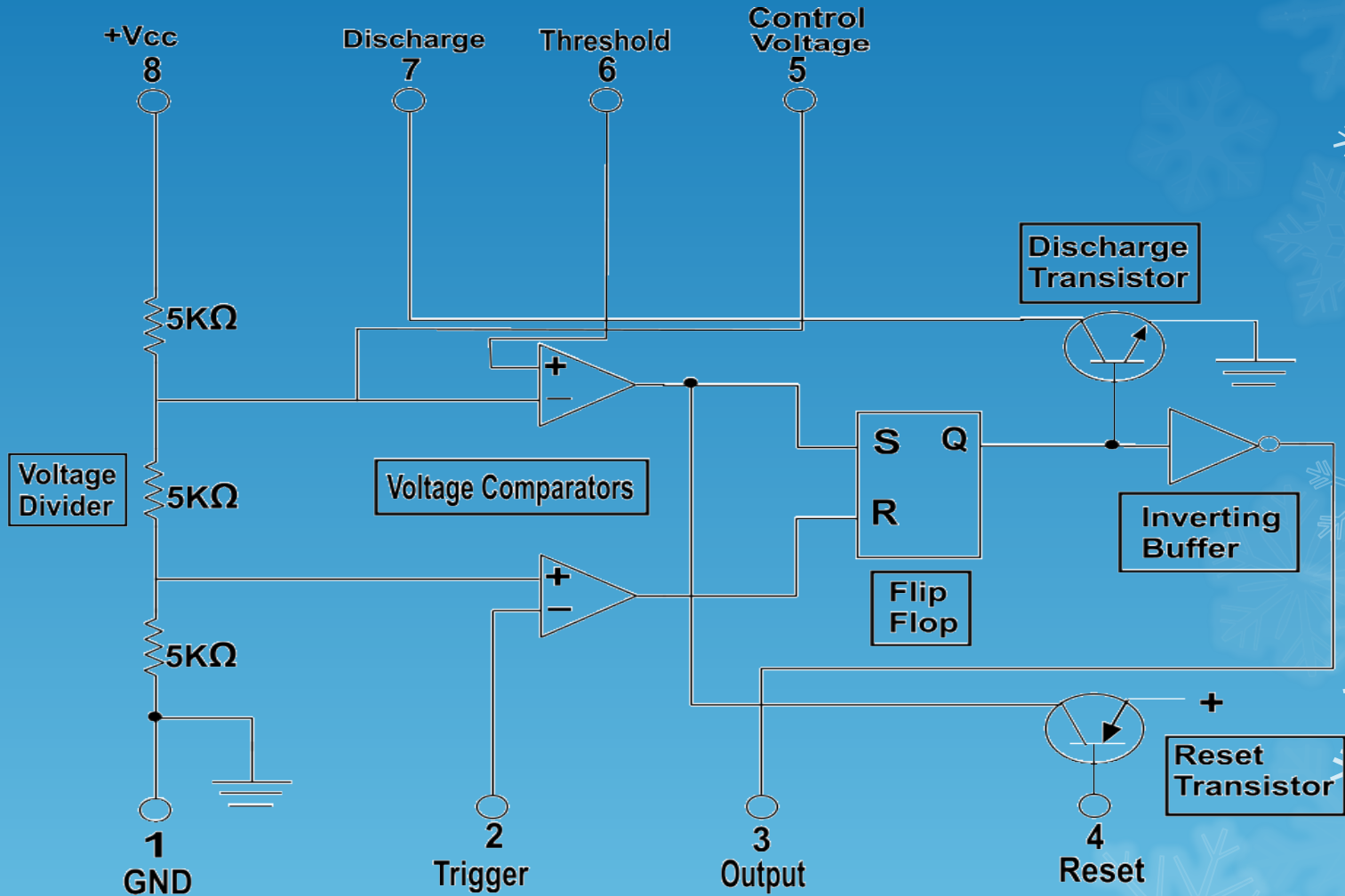


Top View of Metal Can Package



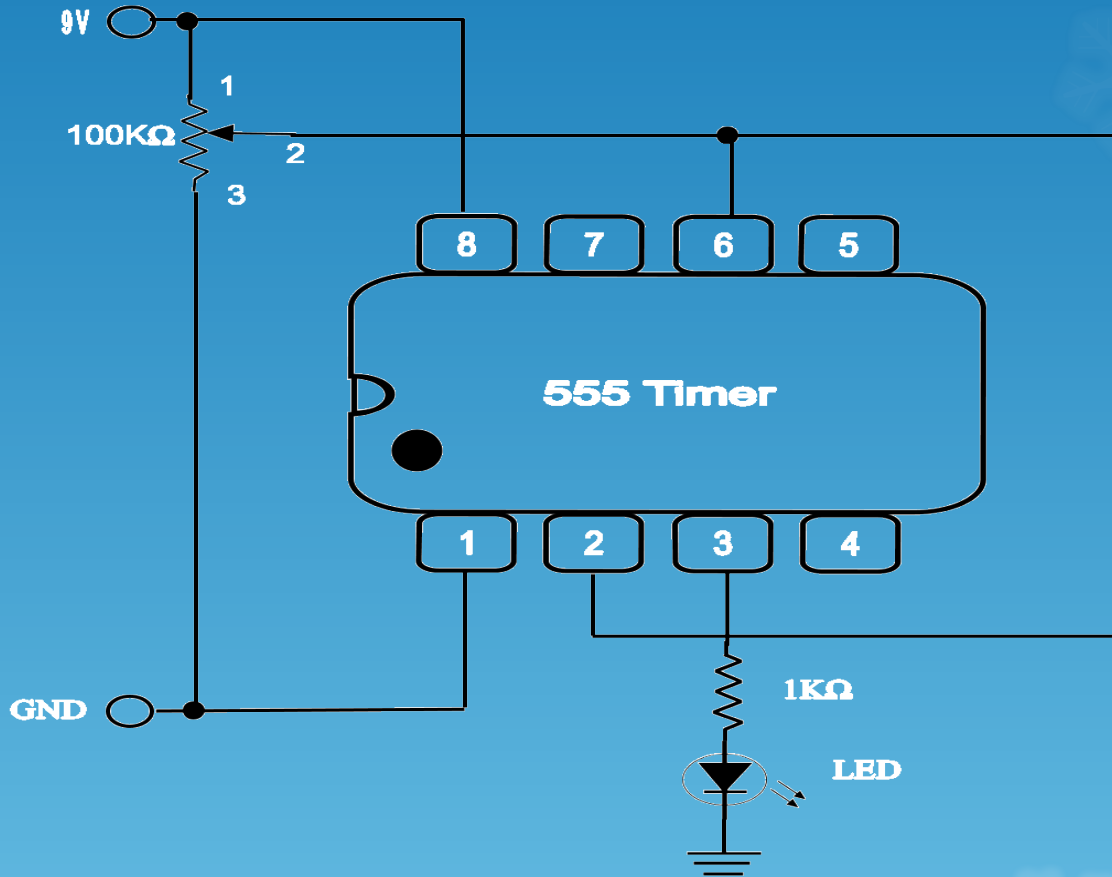
8 Pin DIP (Dual Inline Package)

# 555 Internal Construction Fig 1





# 1456 Fig 2, Experiment 1



# References

- CIE Lesson 1456
- Circuitstoday.com. (2011). *A complete basic tutorial of 555 timer ic.*. Retrieved from [www.circuitstoday.com/555-timer](http://www.circuitstoday.com/555-timer)

# Questions?



# **The End!**

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